

# BLF644P

## Broadband power LDMOS transistor

Rev. 2 — 27 June 2014

Product data sheet

## 1. Product profile

### 1.1 General description

A 70 W LDMOS RF power transistor for broadcast transmitter, communications and industrial applications. The transistor is suitable for the frequency range HF to 1300 MHz. The excellent ruggedness and broadband performance of this device makes it ideal for digital applications.

**Table 1. Typical performance**

RF performance at  $T_{case} = 25\text{ °C}$  in a common source test circuit.

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)	IMD (dBc)
CW, class-A	860	32	100	23	65	-
CW pulsed, class-AB	860	32	100	23.5	66	-
2-tone, class-AB	860	32	45	23	50	-25
	860	32	30	24	40	-35

### 1.2 Features and benefits

- Integrated ESD protection
- Excellent ruggedness
- High power gain
- High efficiency
- Excellent reliability
- Easy power control
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

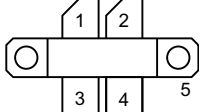
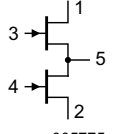
### 1.3 Applications

- Communication transmitter applications in the HF to 1300 MHz frequency range
- Industrial applications in the HF to 1300 MHz frequency range
- Broadcast transmitters



## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		 aaa-005775
2	drain2		
3	gate1		
4	gate2		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF644P	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1228A

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature <a href="#">[1]</a>		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}$ ; $P_L = 90\text{ W}$ <a href="#">[1]</a>	0.75	K/W

[1]  $R_{th(j-c)}$  is measured under RF conditions.

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ ; $I_D = 0.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 32\text{ V}$ ; $I_D = 50\text{ mA}$	1.4	1.9	2.4	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 32\text{ V}$ ; $I_{Dq} = 250\text{ mA}$	1.5	2.0	2.5	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 32\text{ V}$	-	-	1.4	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	-	9.0	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = \pm 10\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	140	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}$ ; $I_D = 2.5\text{ A}$	-	3.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 1.75\text{ A}$	-	300	-	$\text{m}\Omega$

**Table 7. AC characteristics**

$T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 32\text{ V}$ ; $f = 1\text{ MHz}$	-	39	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 32\text{ V}$ ; $f = 1\text{ MHz}$	-	15	-	pF
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 32\text{ V}$ ; $f = 1\text{ MHz}$	-	0.84	-	pF

**Table 8. RF characteristics**

Test signal: CW pulsed, class-AB;  $f = 860\text{ MHz}$ ; RF performance at  $V_{DS} = 32\text{ V}$ ;  $I_{Dq} = 200\text{ mA}$ ;  
 $T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

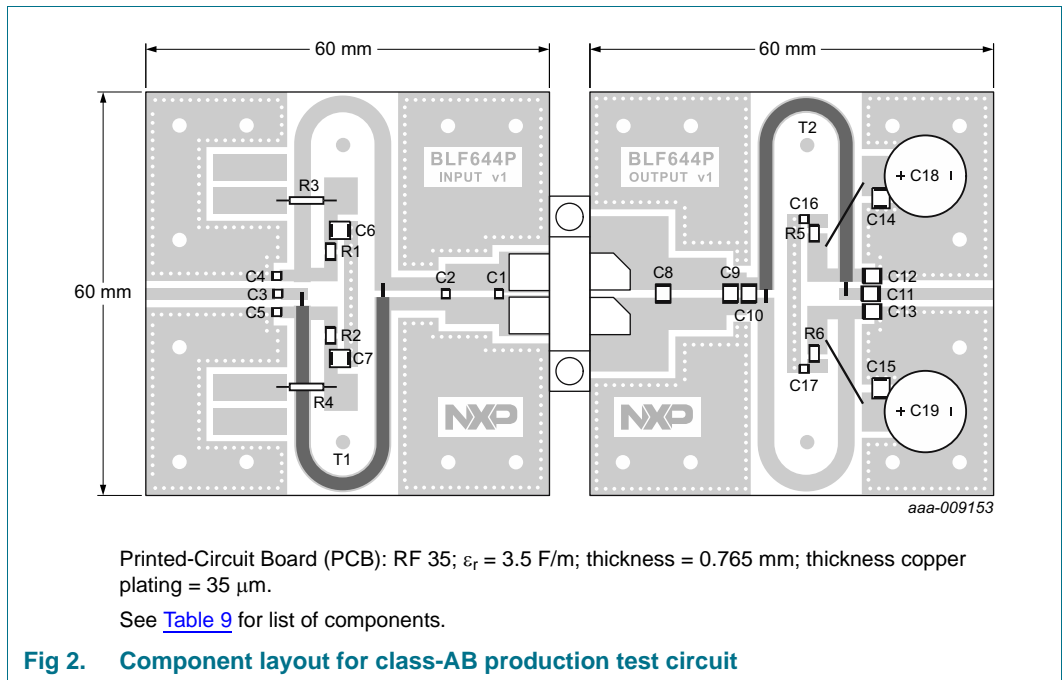
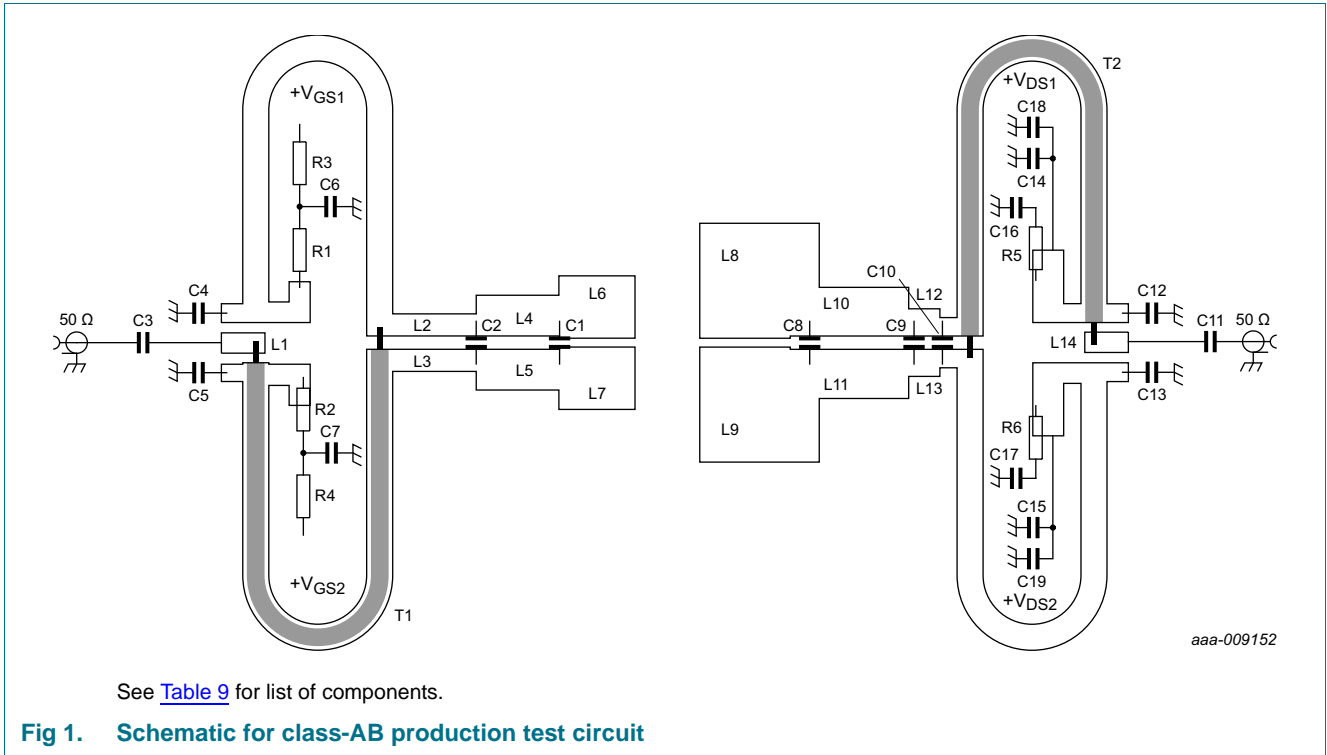
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 100\text{ W}$	22.8	23.5	-	dB
$\eta_D$	drain efficiency	$P_L = 100\text{ W}$	62	66	-	%
$RL_{in}$	input return loss	$P_L = 100\text{ W}$	-	-15	-7	dBc

## 7. Test information

### 7.1 Ruggedness in class-AB operation

The BLF644P is capable of withstanding a load mismatch corresponding to  $VSWR = 10 : 1$  through all phases under the following conditions:  $V_{DS} = 32\text{ V}$ ;  $f = 860\text{ MHz}$  at rated load power.

7.2 Test circuit information



**Table 9. List of components**See [Figure 1](#) and [Figure 2](#).

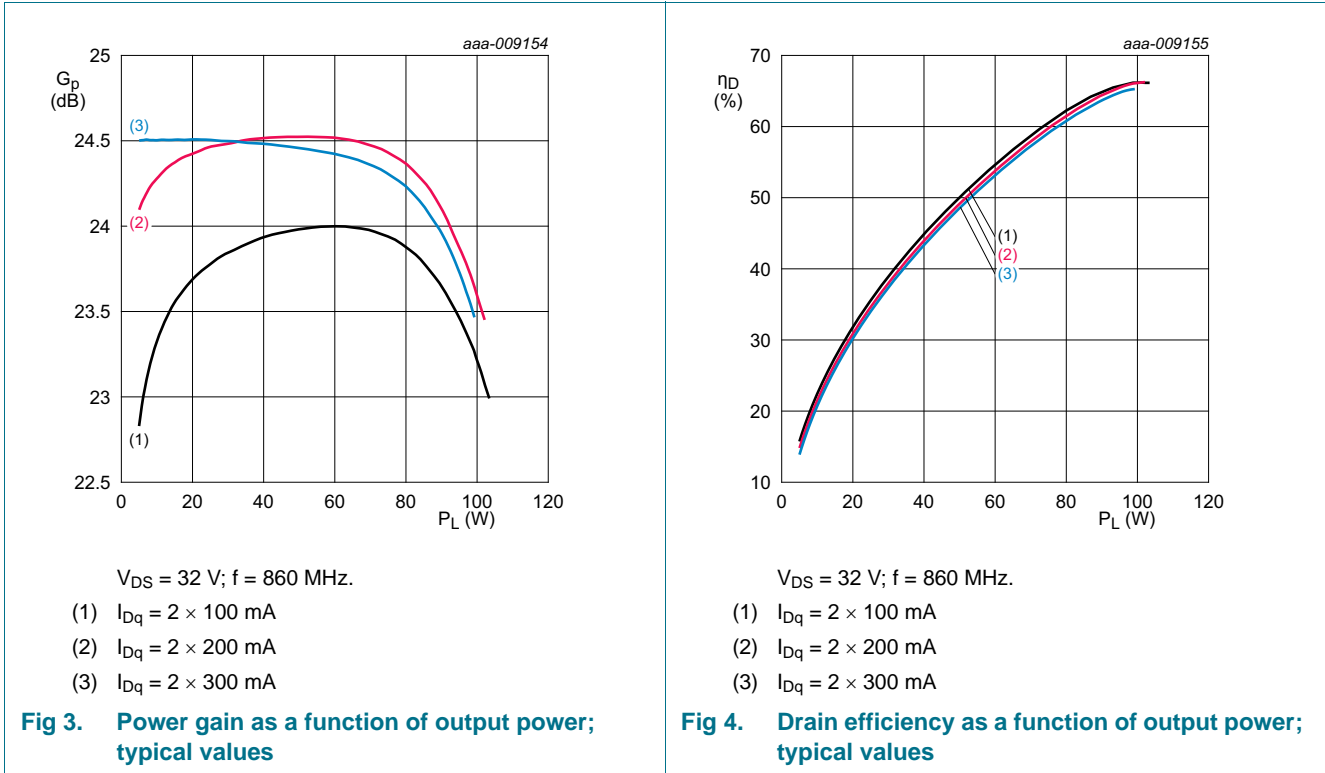
Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	22 pF <a href="#">[1]</a>	
C2	multilayer ceramic chip capacitor	8.2 pF <a href="#">[1]</a>	
C3	multilayer ceramic chip capacitor	62 pF <a href="#">[1]</a>	
C4, C5	multilayer ceramic chip capacitor	51 pF <a href="#">[1]</a>	
C6, C7, C14, C15	multilayer ceramic chip capacitor	4.7 $\mu$ F, 50 V	
C8	multilayer ceramic chip capacitor	12 pF <a href="#">[2]</a>	
C9	multilayer ceramic chip capacitor	5.1 pF <a href="#">[2]</a>	
C10	multilayer ceramic chip capacitor	9.1 pF <a href="#">[2]</a>	
C11	multilayer ceramic chip capacitor	75 pF <a href="#">[2]</a>	
C12, C13	multilayer ceramic chip capacitor	62 pF <a href="#">[2]</a>	
C16, C17	multilayer ceramic chip capacitor	100 pF <a href="#">[1]</a>	
C18, C19	electrolytic capacitor	470 $\mu$ F, 63 V	
L1	microstrip	-	(L $\times$ W) 4 mm $\times$ 1.7 mm
L2, L3	microstrip	-	(L $\times$ W) 8 mm $\times$ 2 mm
L4, L5	microstrip	-	(L $\times$ W) 8 mm $\times$ 4 mm
L6, L7	microstrip	-	(L $\times$ W) 7.4 mm $\times$ 6 mm
L8, L9	microstrip	-	(L $\times$ W) 11.1 mm $\times$ 11.6 mm
L10, L11	microstrip	-	(L $\times$ W) 8.6 mm $\times$ 4.9 mm
L12, L13	microstrip	-	(L $\times$ W) 3 mm $\times$ 2.7 mm
L14	microstrip	-	(L $\times$ W) 4 mm $\times$ 1.7 mm
R1, R2	multilayer ceramic chip capacitor	5.6 $\Omega$	SMD 1206
R3, R4	multilayer ceramic chip capacitor	100 $\Omega$	
R5, R6	multilayer ceramic chip capacitor	30 $\Omega$	SMD 1206
T1, T2	Semi-rigid coaxial cable	25 $\Omega$ , 61 mm	UT-90C-25

[1] American Technical Ceramics type 800A or capacitor of same quality.

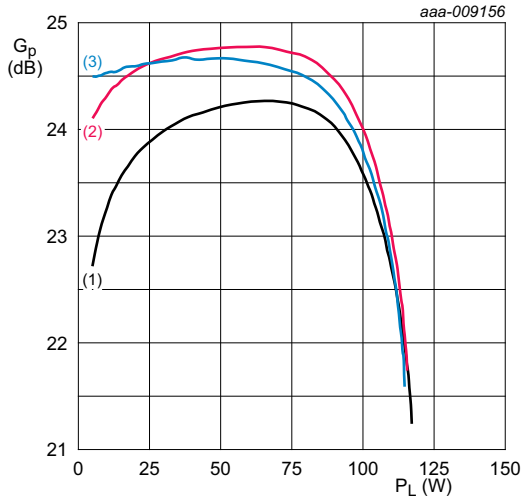
[2] American Technical Ceramics type 800B or capacitor of same quality.

7.3 Graphical data

7.3.1 1-Tone CW

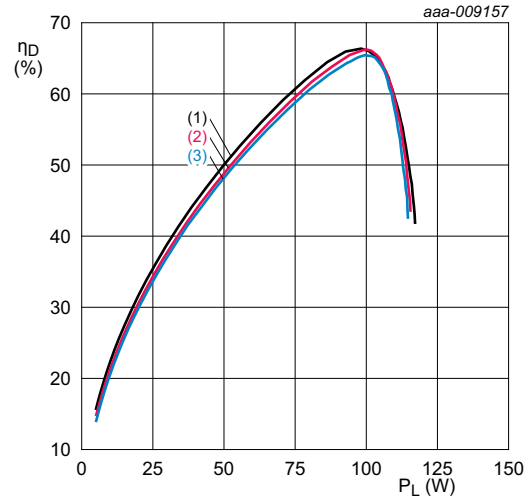


7.3.2 1-Tone pulsed



$V_{DS} = 32\text{ V}; f = 860\text{ MHz}; \delta = 20\%; t_p = 100\ \mu\text{s}.$   
 (1)  $I_{Dq} = 2 \times 100\text{ mA}$   
 (2)  $I_{Dq} = 2 \times 200\text{ mA}$   
 (3)  $I_{Dq} = 2 \times 300\text{ mA}$

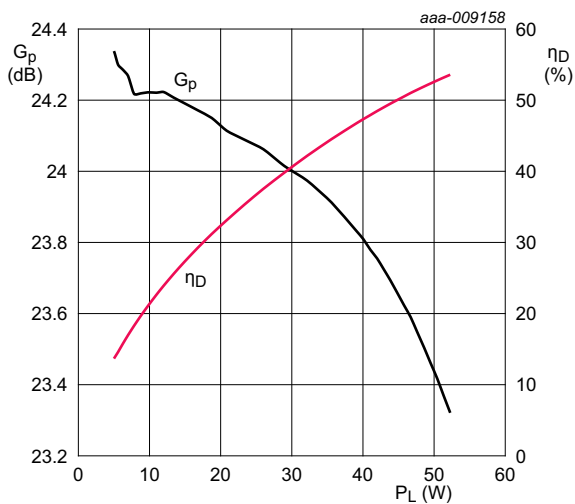
**Fig 5. Power gain as a function of output power; typical values**



$V_{DS} = 32\text{ V}; f = 860\text{ MHz}; \delta = 20\%; t_p = 100\ \mu\text{s}.$   
 (1)  $I_{Dq} = 2 \times 100\text{ mA}$   
 (2)  $I_{Dq} = 2 \times 200\text{ mA}$   
 (3)  $I_{Dq} = 2 \times 300\text{ mA}$

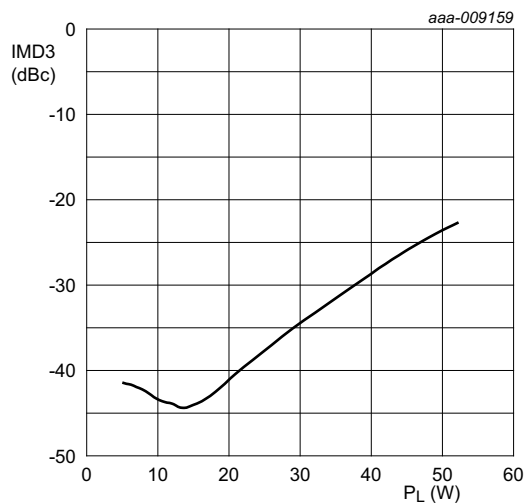
**Fig 6. Drain efficiency as a function of output power; typical values**

7.3.3 2-Tone CW



$V_{DS} = 32\text{ V}; I_{Dq} = 2 \times 350\text{ mA}; f_1 = 889.95\text{ MHz}; f_2 = 890.05\text{ MHz}.$

**Fig 7. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 32\text{ V}; I_{Dq} = 2 \times 350\text{ mA}; f_1 = 889.95\text{ MHz}; f_2 = 890.05\text{ MHz}.$

**Fig 8. Third order modulation distortion as a function of output power; typical values**

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1228A

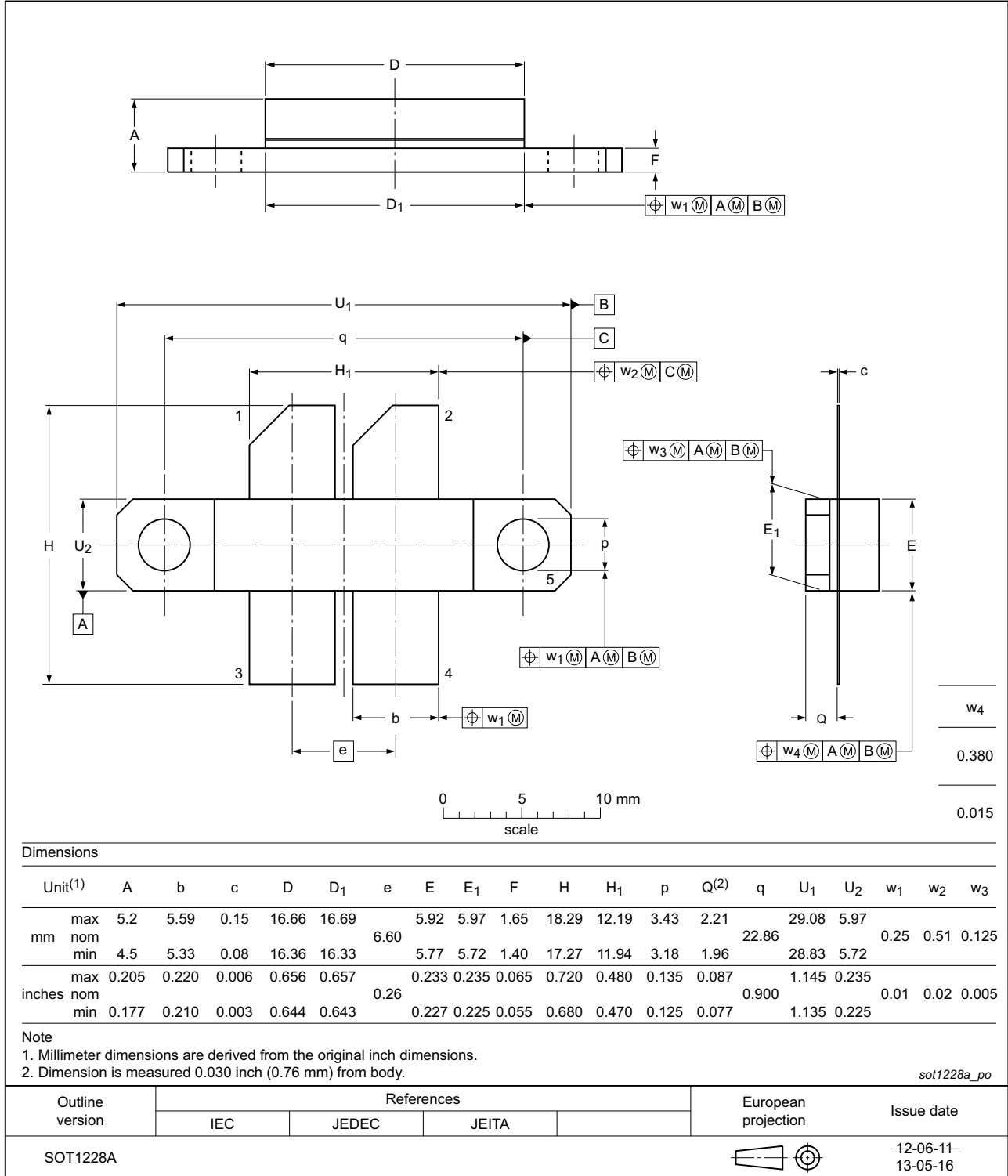


Fig 9. Package outline SOT1228A



## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LDMOST	Laterally Diffused Metal Oxide Semiconductor Transistor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF644P v.2	20140627	Product data sheet	-	BLF644P v.1
Modifications	<ul style="list-style-type: none"> <li>• <a href="#">Section 1.1 on page 1</a>: added 'communications' to the description</li> <li>• <a href="#">Section 1.2 on page 1</a>: added bullet 'broadcast transmitters'</li> <li>• <a href="#">Table 1 on page 1</a>: table has been updated</li> <li>• <a href="#">Table 4 on page 2</a>: table has been updated</li> <li>• <a href="#">Table 5 on page 2</a>: value <math>R_{th(j-c)}</math> set to 0.75 (K/W)</li> <li>• <a href="#">Table 6 on page 3</a>: table has been updated</li> <li>• <a href="#">Table 8 on page 3</a>: table has been updated</li> <li>• <a href="#">Section 7.1 on page 3</a>: value frequency changed from 1300 MHz to 860 MHz</li> <li>• <a href="#">Section 7.2 on page 4</a>: section has been added</li> <li>• <a href="#">Section 7.3 on page 6</a>: section has been added</li> </ul>			
BLF644P v.1	20130611	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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